Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (currently amended) A magnetic semiconductor memory device comprising:

a semiconductor substrate;

first and second word lines arranged in parallel to each other on the semiconductor substrate;

~~a~~ first and second bit ~~line~~ lines crossing the first and second word lines via an insulator layer; and

a first memory cell including a first transistor ~~disposed between~~ controlled by the first word line ~~and the bit line~~ and a first magnetic resistance element disposed between the ~~second word line~~ first transistor and the first bit line;

a second memory cell including a second transistor controlled by the first word line and a second magnetic resistance element disposed between the second transistor and the second bit line;

wherein each of the first and second magnetic resistance ~~element~~ elements is formed into a pillar-like shape by patterning a plurality of layered structures formed on the semiconductor substrate, and at least the side surface is covered with the second word line via the insulator layer,

wherein the magnetic semiconductor memory device further comprises a gap between a first part of the second word line along a side surface of the first magnetic resistance element and a second part of the second word line along a side surface of the second magnetic resistance element.

2. (currently amended) A magnetic semiconductor memory device comprising:

a semiconductor substrate;

first and second word lines arranged in parallel to each other on the semiconductor substrate;

~~a~~ first and second bit ~~line~~ lines crossing the first and second word lines via an insulator layer; ~~and~~

a first memory cell including a first transistor ~~disposed between~~ controlled by the first word line ~~and the bit line~~ and a first magnetic resistance element disposed between the ~~second word line~~ first transistor and the first bit line; and

a second memory cell including a second transistor controlled by the first word line and a second magnetic resistance element disposed between the second transistor and the second bit line;

wherein each of the first and second magnetic resistance ~~element~~ elements is formed into a pillar-like shape by patterning a plurality of layered structures formed on the semiconductor substrate, and the top surface and two side surfaces are covered with the second word line via the insulator layer,

wherein the magnetic semiconductor memory device further comprises a gap between a first part of the second word line along one of the side surfaces of the first magnetic resistance element and a second part of the second word line along one of the side surfaces of the second magnetic resistance element.

3. (original) A magnetic semiconductor memory device as claimed in claim 1, wherein the direction of an electron traveling in a channel area is perpendicular to the main surface of the semiconductor substrate in the transistor.

4. (original) A magnetic semiconductor memory device as claimed in claim 1, wherein a channel is made of polycrystalline silicon in the transistor.

5. (original) A magnetic semiconductor memory device as claimed in claim 1, wherein at least the upper surface of the bit line is covered with a soft magnetic film.

6. (original) A magnetic semiconductor memory device as claimed in claim 1, wherein at least one surface of the second word line is covered with a soft magnetic film.

7. (original) A magnetic semiconductor memory device as claimed in claim 1, wherein the magnetic resistance element is a layered structure including a ferromagnetic material, a tunnel insulator film and a ferromagnetic film.

8. (original) A magnetic semiconductor memory device as claimed in claim 1, wherein the second word line surrounds the bit line in at least three directions via the insulator film.

9. (original) A magnetic semiconductor memory device as claimed in claim 1, wherein the soft magnetic film is permalloy ($Ni_{81}Fe_{19}$).

10. (original) A magnetic semiconductor memory device as claimed in claim 5, wherein the bit line extends between the first and second word lines.

11. (original) A magnetic semiconductor memory device as claimed in claim 1, wherein the bit line extends between the second word line and the magnetic resistance element.

12. (original) A magnetic semiconductor memory device as claimed in claim 1, wherein the magnetic resistance element is formed into a rectangular shape having short sides and long sides, the direction of the long side being perpendicular to the bit line.

13. (currently amended) A magnetic semiconductor memory device comprising:

a semiconductor substrate;

a plurality of word lines formed on the semiconductor substrate;

a plurality of bit lines crossing the plurality of word lines; and

a memory array including memory cells arranged at crossing points between the plurality of word lines and the plurality of bit lines and including a first memory cell and a second memory cell;

wherein each of the memory ~~cell~~ cells includes a vertical type transistor having a channel area formed in a direction perpendicular to the main surface of the semiconductor substrate and having a magnetic resistance element disposed above the vertical type transistor, corresponding one of the plurality of ~~the~~ word ~~line~~ lines being a gate electrode of the vertical type transistor and covering at least two side surfaces of the magnetic resistance element via an insulator film,

wherein gate electrodes of the vertical type transistors included in the first and second memory cells are associated with the same word line,

wherein there is a gap between a first part of the same word line along one side surface of the magnetic resistance element of the first memory cell and a second part of the same word line along one side surface of the magnetic resistance element of the second memory cell.

14. (original) A magnetic semiconductor memory device as claimed in claim 13, wherein at least the upper surface of the bit line is covered with a soft magnetic film.

Claim 15 (cancelled)

16. (original) A magnetic semiconductor memory device as claimed in claim 13, wherein the magnetic resistance element is formed into a rectangular shape having short sides and long sides, the direction of the long side being perpendicular to the bit line.

17. (original) A magnetic semiconductor memory device as claimed in claim 13, wherein a spin flips its direction by varying the direction of a current flowing in the bit line, thus reversing data accordingly.

18. (original) A magnetic semiconductor memory device as claimed in claim 2, wherein the direction of an electron traveling in a channel area is perpendicular to the main surface of the semiconductor substrate in the transistor.

19. (original) A magnetic semiconductor memory device as claimed in claim 2, wherein the second word line surrounds the bit line in at least three directions via the insulator film.

20. (original) A magnetic semiconductor memory device as claimed in claim 2, wherein at least one surface of the second word line is covered with a soft magnetic film.

21. (New) A magnetic semiconductor memory device comprising a magnetic resistance element to which a magnetic field is applied by current flowing in three directions in a single line.

22. (New) The magnetic semiconductor memory device of claim 21, wherein the single line is a word line.

23. (New) The magnetic semiconductor memory device of claim 21, wherein said line surrounds the magnetic resistance element on three sides.